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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,275	06/10/2005	Elstan Anthony Fernandez	1890-0257	9417

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EXAMINER	
PHAM, THANHHA S	
ART UNIT	**PAPER NUMBER**
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,275	FERNANDEZ ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Application is in response to Applicant's Amendment dated 11/5/2006.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 21-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

► With respect to claim 21,

Specification and figures fail to enable to make and/or use invention comprising forming the resin on the first face such that the resin on the first face has a maximum distance from a plane of said substrate which is smaller than a maximum extension of the solder balls from the plane of the substrate.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 16-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

► With respect to claim 16,

It is not clear that "corresponding contacts" are contacts of the substrate or the first intergrated circuit or both?

► With to claim 22,

scope of claim can not be defined since it is not clear that "said region" where the first integrated circuit is located actually having solder balls or not. In addition, it is not clear how "array having a region without solder balls" can have "the solder balls being arranged"

► With respect to claim 26,

lines 1-2, "the electrical contacts" as cited on lines 1-2 of claim 26 refers to which electrical contacts as cited in claim 16. Applicant is respectfully suggested to clarify and use appropriate consistent claimed language wherein different electrical contact should be named differently to define a clear scope of claim.

line 2-3, "electrical contacts on the substrate" renders the claim indefinite. It is not clear that "electrical contacts on the substrate" as cited on lines 2-3 of claim 26 is the same or different electrical contacts as cited on lines 2-3 and/or line 6 in claim 16. Applicant is respectfully suggested to clarify and use appropriate consistent claimed language to define clear scope of claim.

► With respect to claim 27,

It is not clear that “a first face” and "a second face“ are first and second faces of which element.

- With respect to claim 28,

scope of claim can not be defined since it is not clear that "said region" where the first integrated circuit is received actually having solder balls or not. In addition, it is not clear how "array having a region without solder balls” can have “the solder balls being arranged”

- With respect to claim 29,

Lines 3-4, “the electrical contacts electrically connected to corresponding electrical contacts on the substrate” renders the claim indefinite. It is not clear which electrical contacts connected to which electrical contacts. Applicant is respectfully suggested to clarify and use appropriate consistent claimed language wherein different electrical contact should be named differently to define a clear scope of claim.

- With respect to claim 31,

Scope of claim cannot be defined since it is not clear "the electrical contacts" ('s) specifically refer to which electrical contacts. Applicant is respectfully suggested to clarify and use appropriate consistent claimed language wherein different electrical contact should be named differently to define a clear scope of claim.

- With respect to claim 33,

scope of claim can not be defined since it is not clear that "said region" where the first integrated circuit is located actually having solder balls or not. In addition, it is not clear how "array having a region without solder balls" can have "the solder balls being arranged"

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 16-18, 21-22, 27-33, as being best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Choi et al [US 2003/0015782].

► With respect to claims 16-18 and 21-22, Choi et al (figs 2-9b, text [0001]-[0063]) discloses the claimed method of packaging integrated circuits comprising:

attaching a first integrated circuit (30, figs 2 or 3 & figs 5-7b) to a first face (10b) of a substrate (10) with first electrical connections between first electrical contacts (72) of the substrate and first electrical contacts (32) of the first integrated circuit;

attaching a second integrated circuit (20, figs 2 or 3 & figs 5-7b) to a second face (10a) of the substrate with second electrical connections between second electrical

contacts (70) of the substrate and second electrical contacts (22) of the second integrated circuit;

encasing the first and second integrated circuits in resin (molding body 50/52, text [0030]);

wherein the substrate (10, figs 5-7b) includes holes (gate holes) extending between the first face and the second face, the encasing step includes applying the resin to a first side of the substrate and flowing the resin through the holes to the second side of the substrate, whereby the resin forms a single resin body encasing both of the integrated circuits (see fig 7b for details);

wherein, before said encasing step, attaching a box (molding die 220, figs 7a & 7b) to the second side of the substrate defining a volume for receiving the resin;

wherein the substrate is laminar (text [0028] & [0037]-[1038]) and at least the first face includes solder balls (80) arranged in an array on a first region of the first face; wherein the first integrated circuit in located on a second region of the first face.

► With respect to claim 27-28, Choi et al (figs 2-9b, text [0001]-[0063]) discloses the claimed substrate, comprising:

a plurality of first contacts (72) on a first face of the substrate and the first face configured to attach to a first integrated circuit (30) with electrical connection between the first contacts and the first integrated circuit;

a plurality of second contacts (70) on a second face of the substrate and the second face configured to attach to a second integrated circuit (20) with electrical connection between the second contacts and the second integrated circuit;

wherein the substrate defines a plurality of holes (gate holes 16) extending between the first face and the second face, the plurality of holes defining voids configures to pass a resin through the substrate (figs 7a or 7b), the substrate is laminar, and at least the first face includes solder balls (80).

wherein the solder balls are arranged in an array on a first region on the first face, wherein a second region on the first face is configured to receive the first integrated circuit.

► With respect to claims 29-33, Choi et al (figs 2-9b, text [0001]-[0063]) discloses the claimed integrated circuit package substrate, comprising:

a substrate (10) including first electrical contacts (72) on a first side of the substrate and second electrical contacts (70) on a second side of the substrate wherein the first side and the second side are opposite sides;

first and second integrated circuits (20 & 30) attached to the opposite sides of the substrate, wherein first electrical contacts of the first integrated circuit being electrically connected to corresponding the first electrical contacts on the first side of the substrate, wherein second electrical contacts of the first integrated circuit being electrically connected to corresponding the second electrical contacts on the second side of the substrate;

wherein each of the first and second integrated circuits being encased in resin (molding compound 50/52).

wherein a single resin body (fig 7a or 7b, molding compound 250a) encases both of the first and second integrated circuits and extends through holes in the substrate.

wherein at least one of the first and second integrated circuits are respectively connected to the first and second electrical contacts on the substrate by wire bonding.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18-19, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al [US 2003/0015782] in view of Miyajima [US 5,891,384].

► With respect to claim 18, Choi et al substantially discloses the claimed method but is silent about the box including openings defining exit paths for gas within the box.

However, Miyajita (fig 25, cols 1-18) teaches using the box including opening defining exit path (36 or 32) for gas within the box.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Choi et al by using the box as being claimed, per taught by Miyajita to provide a control in process of encasing integrate circuits with resin.

► With respect to claim 20, the claimed pressure for molding operation in the encasing step is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255

(CCPA 1955)., the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> *See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

5. Claims 23-26, 34-35 rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al [US 2003/0015782] in view of Shen [US 6,774,473].

Choi et al substantially discloses the claimed method and integrated circuit package, wherein the first integrate circuit is located in a recessed portion of the substrate and at least one of the first and second integrated circuits are respectively connected to the first and second electrical contacts on the substrate by wire bonding.

Choi et al does not teach using the first integrated circuit comprising a flip chip.

However, using the flip chip in integrated circuit connection to the substrate has been known in the art. Moreover, Shen shows equivalence of using the integrated circuit of Choi et al to the using of the integrated circuit of flip chip.

Therefore, at the time of invention, it would have been obvious for those skill in the art, in view of Shen, to select flip chip for the first intergated circuit in the process/package of Choi et al as a convenient choice of integrated circuit to provide appropriate function in device.

In regarding to claims 25 and 35, combination of teaching of Shen to process/package of Choi et al would provide the flip chip in the recessed portion of the substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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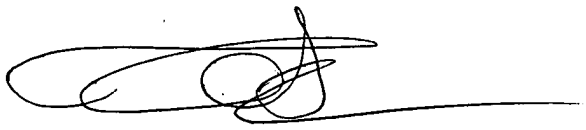

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